REMARKS

Applicants note with appreciation the allowance of claim 20. Claims 1-21 are pending in the present application.

Claims 1-7 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentble over U.S. Patent No. 6,200,855 (Lee) in view of Moise et al. (Although the Office Action did not specify the U.S. Patent number for Moise et al., U.S. Patent No. 6,534,809 was used in a prior Office Action and all remarks referring to Moise et al. herein will be based on U.S. Patent No. 6,534,809.) Applicants respectfully traverse this rejection.

The claimed invention relates to forming metal plugs in a peripheral logic circuitry area of a semiconductor device to contact regions of differently doped conductivity, e.g., both N and P doped regions, of transistors in the peripheral logic circuitry area. The metal plugs are formed after all high temperature processing is completed, such that the metal does not diffuse into the active areas of the substrate. As such, claim 1 recites a method of forming a memory device comprising the steps of "forming at least a portion of a capacitor structure . . .; heat treating said capacitor structure; and forming metal plugs down to active areas of a substrate after heat treating said capacitor structure, wherein at least a portion of said metal plugs formed down to said active areas are for both N-channel and P-channel peripheral logic transistors of a semi-conductor substrate located outside said memory array area containing said memory cell."

Similarly, claim 2 recites a method of forming a memory device comprising the steps of "forming a lower electrode layer of a memory cell capacitor; forming a dielectric layer . . .; heat treating said lower electrode and dielectric layer; after said heat treating operation, forming an upper electrode layer . . .; and . . . forming metal contacts contiguous to active areas of each of an N-channel and P-channel transistor in a peripheral logic area."

Claim 3 recites a method of fabricating metallized plugs in a memory device by, *inter alia*, forming a capacitor, "applying heat to anneal said capacitor; defining multiple plug openings in material layers over said substrate at said periphery circuitry area of said substrate, wherein at least one of said plug openings exposes an active area of said transistor having said first conductivity type and at least one of said plug openings exposes an active area of said transistor having said second conductivity type; and forming a metal layer over said substrate and into said plug openings to contact said active areas after said heat is applied to said memory cell array area."

Claim 6 recites a method of forming a memory device comprising, *inter alia*, the steps of "forming container capacitors, respectfully associated with one of said access transistors in said second insulating layer over and in electrical communication with respective capacitor polysilicon plugs; heat treating said container capacitors; forming N-channel and P-channel peripheral logic transistors outside said memory cell array area; after said heat treating, forming metal plugs to contact each of said N-channel and P-channel peripheral logic transistors through said first and second insulating layer."

Claim 7 recites a method of forming a memory device comprising, *inter alia*, the steps of "forming at least portions of capacitors associated with said access transistors in said memory cell array area; heat treating said capacitor portions; and after said heat treating, forming first metal conductors which contact with active areas of said N-channel and P-channel peripheral logic transistors." Lee and Moise et al., whether taken alone or in combination, do not teach or suggest all the limitations of the claimed invention.

Lee relates to a method of forming a semiconductor memory device "which can reduce the contact resistance between the p+ impurity region and metal line." (Col. 3, lines 18-20). Lee discloses that "a patterning is carried out to form a storage node, i.e., a lower electrode 122 of the capacitor." (Col. 6, lines 21-22; Fig. 2C). Lee further discloses that a "dielectric layer 124 and an upper capacitor electrode 125 are formed, thereby completing the formation of a capacitor." (Col. 6, lines 24-26; Fig. 2C). Lee then

discloses forming a fourth insulating layer 126 on the entire surface of the semiconductor substrate 100 before etching the fourth insulating layer 126, the third insulating layer 118, the mask nitride layer 116b, the second insulating layer 112, and the first insulating layer 109 "until the p+ impurity region 106b . . . [is] exposed, thereby forming contact holes 128a to 128c." (Col. 6, lines 30-41; Fig. 2C). Lee also discloses that the "contact holes 128a to 128c are filled with a metal." (Col. 6, lines 50-51).

Lee does not teach or suggest all the limitations of the claimed invention. Specifically, Lee is silent on, *inter alia*, "forming metal plugs down to active areas of a substrate after heat treating said capacitor structure," as recited in claim 1; "after said heat treating operation, forming an upper electrode layer," as recited in claim 2; "forming a metal layer over said substrate and into said plug openings to contact said active areas after said heat is applied to said memory cell array area," as recited in claim 3; and "after said heat treating, forming first metal conductors which contact with active areas of said N-channel *and* P-channel peripheral logic transistors," as recited in claim 7 (emphasis added). By contrast, Lee is silent on heat treating the capacitor structure prior to forming metal conductors. Moreover, Lee only forms metal conductors which contact the p+ impurity region, not both N-channel and P-channel peripheral logic transistors as in the claimed invention.

Moise et al. cannot supplement the inadequacies of Lee. Moise et al. relates to a method of forming a ferroelectric memory (FeRAM). Moise et al. discloses a method of "creating the ferroelectric capacitors in a FeRAM process module that occurs between the front end module (defined to end with the formation of tungsten . . .) and backend process module (mostly metallization)." (Col. 4, lines 55-59). Moise et al. discloses etching a dielectric layer 112 "to form openings for contacts to the subsrate and gate structures . . . filled with one or more conductive materials, such as plug 114." (Col. 7, lines 39-46; Fig. 1). Moise et al. further discloses that the "bottom electrode 124 of capacitor 125 is formed (step 206) either on barrier layer barrier layer 122 or directly on layer 112 so as to make electrical connection with the underlying contact structure . . .. The capacitor

dielectric is formed (step 208) on the bottom electrode. . . . The top electrode is formed (step 210) on the capacitor dielectric 126." (Col. 9, line 27 – Col. 10, line 28; Figs. 1-2). Moise et al. also discloses that in a "step 222 and prior to the conductor 132 and liner 138 formation, the anneal of the instant invention is performed so as to remove damage introduced by the capacitor stack processing." (Col. 20, lines 38-41; Figs. 1-2).

First, there is no motivation to combine Moise et al. with Lee. Moise et al. relates to FeRAM memory, which is non-volatile memory, whereas Lee relates to dynamic random access memory, which is volatile and requires N- and P-channel transistors for peripheral circuitry. Furthermore, there is nothing in Moise et al. or Lee to suggest that their teachings may be modified with the teachings of the other. Thus, one ordinarily skilled in the art would not have been motivated to modify the teachings of Lee with those of Moise et al. to obtain the claimed invention.

Second, even assuming, *arguendo*, there exists a motivation to combine Moise et al. with Lee (which there is not), the references do not teach or suggest all the limitations of the claimed invention. Moise et al., like Lee, fails to teach or suggest all the limitations of the claimed invention. Specifically, Moise et al. is silent on, *inter alia*, "forming metal plugs down to active areas of a substrate after heat treating said capacitor structure, wherein at least a portion of said metal plugs formed down to said active areas are for both N-channel and P-channel peripheral logic transistors," as recited in claim 1; "after forming said upper electrode layer, forming metal contacts contiguous to active areas of each of an N-channel and P-channel transistor in a peripheral logic area," as recited in claim 2; "defining multiple plug openings in material layers over said substrate at said periphery circuitry area of said substrate, wherein at least one of said plug openings exposes an active area of said transistor having said first conductivity type and at least one of said plug openings exposes an active area of said transistor having said second conductivity type," as recited in claim 3; "after said heat treating, forming metal plugs to contact each of said N-channel and P-channel peripheral logic transistors through said first and second insulating layer," as recited in claim 6; and "after said heat treating, forming first metal conductors

which contact with active areas of said N-channel and P-channel peripheral logic transistors," as recited in claim 7.

By contrast, Moise et al. discloses adding a layer 127 to accommodate the FeRAM cells and etching an opening in ILD layer for metal plugs 136. (Col. 8, lines 29-50). The metal plugs 136 of Moise et al. that are formed after the capacitors are formed *contact other conductive plugs 114*, and not *the active areas of the N-channel and P-channel transistors.* Furthermore, as discussed above, Moise et al. is directed to a method of forming FeRAM cells which *do not have a transistor having a first conductivity type and a transistor having a second conductivity type in a peripheral circuitry area*, as in the claimed invention. Since Lee and Moise et al., whether taken alone or in combination, do not teach or suggest all the limitations of claims 1-3, 6 and 7, these claims and dependant claims 4-6 and 9 are patentable over the references. For at least these reasons, Applicants respectfully request the withdrawal of the 35 U.S.C. § 103(a) rejection of claims 1-7 and 9.

Claims 1-5, 7 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,858,831 (Sung) in view of Moise et al. Applicants respectfully traverse this rejection.

Claim 21 recites a method of forming a metallized contact to a periphery transistor, comprising, *inter alia*, "annealing said capacitor structures by applying heat to at least one of said bottom layer, said dielectric layer, or said capacitor plate; after annealing said capacitor structure, etching through said second insulating layer to define peripheral plug openings in said peripheral array area to expose active areas of said first and second conductivity type; and depositing a metal layer over said substrate to form metal plugs in said peripheral array area to contact respective active areas of said first conductivity type and said second conductivity type." Sung and Moise et al., whether taken in alone or in combination, do not teach or suggest all the limitations of the claimed invention.

Sung relates to "a process used to fabricate high performance logic devices and low cost memory devices, on a single semiconductor chip." (Col. 1, lines 8-10). Sung

discloses forming a storage node of a capacitor structure in a DRAM region 60, then forming metal contacts 45 and 46 in the logic region 50 by etching contact holes 42 and 43 in silicon oxide layers 29 and 34. (Col. 7, line 45 – Col. 8, line 45; Figs. 18-20). Sung is completely silent on annealing or heat treating the capacitor structures prior to forming metal plugs, as in the claimed invention.

Moise et al. cannot supplement the inadequacies of Sung in this respect. There is no motivation to combine the teachings of Sung with the teachings of Moise et al. Sung provides a process for fabricating embedded DRAM memory devices and high performance CMOS logic devices on the same semiconductor chip, whereas, as mentioned above, Moise et al. is directed to a method of forming FeRAM cells. Furthermore, there is nothing in Moise et al. or Sung to suggest that their teachings may be modified with the teachings of the other. Thus, one ordinarily skilled in the art would not have been motivated to modify the teachings of Sung with those of Moise et al. to obtain the claimed invention. As also discussed above, Moise et al., alone, fails to teach or suggest all the limitations of the claimed invention.

Therefore, Sung and Moise et al. do not teach or suggest, *inter alia*, "forming metal plugs down to active areas of a substrate after heat treating said capacitor structure, wherein at least a portion of said metal plugs formed down to said active areas are for both N-channel and P-channel peripheral logic transistors," as recited in claim 1; "after forming said upper electrode layer, forming metal contacts contiguous to active areas of each of an N-channel and P-channel transistor in a peripheral logic area," as recited in claim 2; "defining multiple plug openings in material layers over said substrate at said periphery circuitry area of said substrate, wherein at least one of said plug openings exposes an active area of said transistor having said first conductivity type and at least one of said plug openings exposes an active area of said transistor having said second conductivity type," as recited in claim 3; "after said heat treating, forming first metal conductors which contact with active areas of said N-channel and P-channel peripheral logic transistors," as recited in claim 7; and "after annealing said capacitor structure, etching through said second

insulating layer to define peripheral plug openings in said peripheral array area to expose active areas of said first and second conductivity type," as recited in claim 21. Since Sung and Moise et al. do not teach all the limitations of claims 1-3, 7 and 21, these claims and dependant claims 4-5 are patentable over the references. For at least these reasons, Applicants respectfully request the withdrawal of the 35 U.S.C. § 103(a) rejection of claims 1-5, 7 and 21.

Claims 1-5, 7-9, 11-14 and 17-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,893,734 (Jeng et al.) in view of Moise et al. Applicants respectfully traverse this rejection.

Claim 18 recites a method of forming a memory device comprising, *inter alia*, "forming container capacitors, respectfully associated with each of said access transistors in said second insulating layer over and in electrical communication with respective capacitor polysilicon plugs; heat treating said container capacitors; forming N-channel and P-channel peripheral logic transistors outside said memory cell array area; forming peripheral metal plugs through said second insulating layer to contact each of said N-channel and P-channel peripheral logic transistors after said heat treating." Jeng et al. and Moise et al., whether taken alone or in combination, do not teach or suggest all the limitations of the claimed invention.

Jeng et al. relates to a method of fabricating of DRAM devices "with an array of memory cells having capacitor-under-bit line (CUB)." (Col. 1, lines 10-14). Jeng et al. discloses that "Si_3N layer 24 is removed over the source/drain contact areas 19 (N+) in the exposed contact openings 2, 2' and 2''. . . [and] a conformal conductively doped polysilicon layer 32 is deposited." (Col. 6, lines 44-48; Fig. 5). Jeng et al. further discloses "forming conductive plugs 38' composed of tungsten with a barrier layer of $TiN/TiSi_2$ . . . [to] serve as landing plug contacts for the multilevel contact openings that are formed later." According to Jeng et al., capacitors are then formed, including bottom electrodes 46', dielectric layer 50 and conformal third conducting layer 52, before forming

a fourth insulating layer 43, and "etching multilevel contact openings 7' in the fourth insulating layer 32 . . . to the landing plug contacts 38' on the patterned polycide layer (18, 16) in the peripheral device are 9." (Col. 8, lines 26-59; Figs. 11-12). Jeng et al. fails to suggest annealing or heat treating the capacitors and forming metal plugs to any transistor, much less forming metal plugs or contacts to a peripheral logic transistor after heat treatment of a capacitor structure.

For at least the same reasons as discussed above regarding the combination of Moise et al. with Sung and Lee, Moise et al. cannot supplement the inadequacies of Jeng et al. in this respect. There is no motivation to combine the teachings of Jeng et al. with the teachings of Moise et al. since Jeng et al. provides a method for fabricating DRAM devices, whereas, Moise et al. is directed to a method of forming FeRAM cells. Furthermore, there is nothing in Moise et al. or Jeng et al. to suggest that their teachings may be modified with the teachings of the other. Therefore, one ordinarily skilled in the art would not have been motivated to modify the teachings of Jeng et al. with those of Moise et al. to obtain the claimed invention. Even assuming, *arguendo*, that Moise et al. could be combined with Jeng et al., the metal plugs of Moise et al. formed after the formation of the capacitors contact other conductive plugs, and not the active areas of the transistors having a first conductivity type and the transistors having a second conductivity type. Therefore, Moise et al. fails to teach or suggest forming peripheral metal plugs through a second insulating layer to contact a peripheral logic transistor after said heat treating, as taught by the claimed invention.

Since Sung and Moise et al. do not teach all the limitations of claims 1-3, 7 and 18, these claims and dependant claims 4-5, 8-9, 11-14, 17 and 19 are patentable over the references. For at least these reasons, Applicants respectfully request the withdrawal of the 35 U.S.C. § 103(a) rejection of claims 1-5, 7-9, 11-14 and 17-19.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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